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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,704	10/31/2003	Robert O. Conn	X-1416-3 US	1939

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,704	CONN, ROBERT O.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 12-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/29/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/698704 Attorney's Docket #: X-1416-3US
Filing Date: 10/31/2003;

Applicant: Conn Examiner: Alexander Williams

Applicant's Response filed 12/12/07 to the election of Group I (claims 1 to 8 and 12 to 16) filed 6/29/05 to the species elected of species of figures 1 to 7 filed 4/4/05 has been acknowledged.

Claims 9-11 have been cancelled.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite to the first position and to a second landing pad in the array of landing pads in claim 1 and the means for coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed opposed the first position and to a second landing pad located in a different position in the array of landing pads in claim 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 1 to 8 and 12 to 16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1 and similar claim 12, it is unclear and confusing to what is meant by and what shows "the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite to the first position and to a second landing pad in the array of landing pads." Understanding this, with the interposer 203 coupling a first micro-bump (one of the integrated circuit die having an array of micro-bumps) in a first position (where the micro-bump sits in the array of micro-bumps) in the array of micro-bumps (from the integrated circuit die 102) to a first landing pad (pad on the interposer lined with the first position) located opposite to the first position and to a second landing pad (another pad) in the array of landing pads (array of landing pads of the integrated circuit package 101), how is interposer coupling this first micro-bump to a first landing pad and the second landing pad with the description of the positions of the other elements claimed? Please explain the claimed structure as it relates to the drawings and specification so the examiner can better

understand what is being claimed. How is one element (a first micro bump) connected to a first landing pad at on location and to a second landing pad location at another position?

Any of claims 1 to 8 and 12 to 16 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1- 8 and 12-16**, insofar as they can be understood**, are rejected under 35 U.S.C. 102(e) as being anticipated by Chung et al. (U.S. Patent # 6,680,218 B2).

1. Chung et al. (figures 1 to 11) specifically figure 5 show an assembly, comprising: an integrated circuit die **302** having an array of micro-bumps **(bumps between 302 and 304)** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **306** having an array of landing pads **(pads on the top surface of 306)** disposed on an inside surface of the integrated circuit package in a second pattern and array of solder balls **142**

disposed on an outside surface of the integrated circuit package, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure **304** disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad (pads not labeled but shown) located opposite to the first position and to a second landing pad **(pads not labeled but shown)** in the array of landing pads.

2. The assembly of claim 1, Chung et al. show wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit does not extend through the second landing pad of the integrated circuit package.
3. The assembly of claim 2, Chung et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.
4. The assembly of claim 3, Chung et al. show wherein the interposing structure includes no transistor and no PN junction.
5. The assembly of claim 4, Chung et al. show wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.
6. The assembly of claim 5, Chung et al. show wherein the interposing structure includes a layer comprising epoxy and fiberglass.

7. The assembly of claim 5, Chung et al. show wherein the interposing structure includes a bypass capacitor **308**.

8. The assembly of claim 5, Chung et al. show wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor disposed in the interposing structure extends in a direction parallel to the surface of the integrated circuit.

12. Chung et al. (figures 1 to 11) specifically figure 5 show an assembly, comprising: an integrated circuit die **302** having an array of micro-bumps **(bumps between 302 and 304)** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **306** having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; the means **304** for coupling a first micro-bump in a first position in the array of microbumps to a first landing pad disposed opposed the first position and to a second landing pad located in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

13. The assembly of claim 12, Chung et al. show wherein the interposing structure includes a bypass capacitor **308**.

14. The assembly of claim 12, Chung et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. The assembly of claim 12, Chung et al. show wherein the means has a planar form and is less than 500 microns thick.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. The assembly of claim 12, Chung et al. show wherein the integrated circuit die is an application specific integrated circuit (ASIC).

(5) IC 302 could be any of a number of types of ICs. In one embodiment of the present invention, IC 302 is a microprocessor, although IC 302 could be an application specific integrated circuit (ASIC), memory device or many other types of devices in other embodiments.

Claims 1- 8 and 12-15, **insofar as they can be understood**, are rejected under 35 U.S.C. 102(b) as being anticipated by Chance et al. (U.S. Patent # 5,177,594).

1. Chance et al. (figures 1 to 21) specifically figures 1and 4 show an assembly, comprising: an integrated circuit die **52** having an array of micro-bumps **56** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **54** having an array of landing pads **(inherent (see figure 4 pads above and below elements 90,78 with 92))** disposed on an inside surface of the integrated circuit package in a second pattern and array of solder balls **(pins)** disposed on an outside surface of the integrated circuit package, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure **50** disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad (pads not labeled but shown) located opposite to the first position and to a second landing pad **(inherent (see figure 4 lower bonding pads on elements 78,90))** in the array of landing pads.

2. The assembly of claim 1, Chance et al. show wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit does not extend through the second landing pad of the integrated circuit package.

3. The assembly of claim 2, Chance et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.

4. The assembly of claim 3, Chance et al. show wherein the interposing structure includes no transistor and no PN junction.

5. The assembly of claim 4, Chance et al. show wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.

6. The assembly of claim 5, Chance et al. show wherein the interposing structure includes a layer comprising epoxy and fiberglass.

7. The assembly of claim 5, Chance et al. show wherein the interposing structure includes a bypass capacitor **(see figures 9 and 10)**.

8. The assembly of claim 5, Chance et al. show wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor disposed in the interposing structure extends in a direction parallel to the surface of the integrated circuit.

12. Chance et al. (figures 1 to 21) specifically figure 1 show an assembly, comprising: an integrated circuit die **52** having an array of micro-bumps **56** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **54** having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; the means **50** for coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed opposed the first position and to a second landing pad located in a different position in the array of landing pads, the means being disposed inside the

integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

13. The assembly of claim 12, Chance et al. show wherein the interposing structure includes a bypass capacitor **(see figures 9 and 10)**.

14. The assembly of claim 12, Chance et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. The assembly of claim 12, Chance et al. show wherein the means has a planar form and is less than 500 microns thick.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response

Applicant's arguments filed 12/12/07 have been fully considered, but are moot in view of the new and outstanding grounds of rejections detailed above. Applicant's arguments states "Chung does not teach or suggest an interposer that couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package" is not found to be persuasive. The language of "each of which being on inside surface of an integrated circuit package" is not claimed structure.

Applicant's arguments stating "There is no teaching or suggesting in Chung that one of the solder bumps on the IC 302 is coupled to both a bond pad opposite the solder bump and another bond pad on the horizontal section" in not found to be persuasive. Chung does show the element 516 in figure 5 coupling the two bond pads.

Applicant's arguments stating "Chance does not teach or suggest an interposer that couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package" is not found to be persuasive. The language of "each of which being on inside surface of an integrated circuit package" is not claimed structure.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., each of which being on inside surface of an integrated circuit package) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/653,758,774,778,737,738,734,686,685,723,691,774,6 92,693,700,e25.013,e23.125,e23.079,e23.026,e23.e23.06 3.e23.101,e23.181,e23.069,e23.126,e23.067,e23.062 361/306.3,312,313,321.1,321.4,763,748,762,760	9/11/05 4/13/06 7/24/06 12/23/06 9/13/07 2/26/08
Other Documentation: foreign patents and literature in 257/653,758,774,778,737,738,734,686,685,723,691,774,6 92,693,700,e25.013,e23.125,e23.079,e23.026,e23.e23.06 3.e23.101,e23.181,e23.069,e23.126,e23.067,e23.062 361/306.3,312,313,321.1,321.4,763,748,760,762	9/11/05 4/13/06 7/24/06 12/23/06 9/13/07 2/26/08
Electronic data base(s): U.S. Patents EAST	9/11/05 4/13/06 7/24/06 12/23/06 9/13/07 2/26/08

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Alexander O Williams/
Primary Examiner, Art Unit 2826

AOW
3/13/2008